PATENT APPLICATION
Docket No. 1482-132

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Barrie Gilbert

Serial No.:	09/545,691	Examiner:	Philip Sobutka
Filed:	April 7, 2000	Group Art Unit:	2684
For:	RF MIXER WITH INDUCTIVE DEGENERATION		
Date:	June 13, 2006		

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUBSTITUTE APPEAL BRIEF

This Appeal Brief is in response to the Notification of Non-Compliant Appeal Brief mailed in this case on May 30, 2006. Appeal is taken from the Examiner's Final Office Action mailed June 4, 2004 finally rejecting claim 15.

REAL PARTY IN INTEREST

The present application has been assigned to the following party:

Analog Devices, Inc.
One Technology Way
Norwood, MA 02062

RELATED APPEALS AND INTERFERENCES

The Board's decision in the present Appeal will not directly affect, or be directly affected, or have any bearing on any other appeals or interferences known to the appellant, or to the Applicant's legal representative.

STATUS OF CLAIMS

Claims pending in the application: 2-3, 9-10, 13 and 15-26

Claims drawn to allowable subject matter: 2-3, 9-10, 13 and 16-26

Claims rejected: 15 (which is finally rejected)

Claims appealed: 15

STATUS OF AMENDMENTS

No amendments have been filed subsequent to final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Claim 15 recites an amplifier cell having two input terminals and two output terminals. The cell includes two class AB input stages, each of which drives both of the output terminals in response to an input signal received at one of the input terminals. An example embodiment of such an amplifier is shown in Fig. 26. In the circuit of Fig. 26, transistors Q1, Q2 and Q3 form a first class AB input stage that drives the output terminals 38 and 40 in response to a first input signal V_{IN1}. Transistors Q4, Q5 and Q6 form a second class AB input stage that drives the output terminals 38 and 40 in response to a second input signal V_{IN2}. See page 20, lines 24-29.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claim 15 is unpatentable under 35 U.S.C. 103(a) based on U.S. Patent No. 5,789,799 to Voinigescu et al. ("Voinigescu") in view of U.S. Patent No. 5,307,512 to Mitzlaff ("Mitzlaff").

ARGUMENT

The present patent application discloses amplifiers having, among other things, several types of input stages that drive two output terminals responsive to a single input signal. An example embodiment of such an input stage is shown as item 26 in Fig. 3 where transistors Q11, Q12 and Q13 form a class AB input stage that drives output terminals 38 and 40 in response to a signal received at input terminal 44.

The invention recited in claim 15 takes this concept a step further by combining two class AB input stages to drive the output terminals in response to two input signals, thus providing

fully differential operation. An example embodiment of such an amplifier is shown in Fig. 26. In the circuit of Fig. 26, transistors Q1, Q2 and Q3 form a first class AB input stage that drives the output terminals 38 and 40 in response to a first input signal V_{IN1}. Transistors Q4, Q5 and Q6 form a second class AB input stage that drives the output terminals 38 and 40 in response to a second input signal V_{IN2}.

Claim 15 reads as follows:

15. An amplifier cell comprising:

first and second input terminals;

first and second output terminals;

first class AB input stage coupled to the first and second output terminals and arranged to drive the first and second output terminals responsive to a first input signal received at the first input terminal; and

a second class AB input stage coupled to the first and second output terminals and arranged to drive the first and second output terminals responsive to a second input signal received at the second input terminal.

Thus, claim 15 recites two input stages of a specific type that are arranged in a well-defined manner.

In the Office Action (paper No. 20) mailed December 12, 2003, the examiner rejected claim 15 and identified specific circuit elements in the Voinigescu reference alleged to satisfy elements recited in claim 15. However, the Examiner's arguments with respect to the prior art are incorrect in terms of (1) what the elements are, and (2) how the elements are arranged.

Claim 15 recites a second class AB input stage. The Examiner alleges that transistors Q3 and Q6 in Fig. 9 of Voinigescu, although not a class AB circuit, still satisfy the requirement of an "input stage." However, the Voinigescu reference does not support this interpretation. Transistors Q3 and Q6 are not an "input stage," but instead are part of a "mixing quad" formed by transistors Q3, Q4, Q5 and Q6. (See col. 14, lines 31-32 of Voinigescu.)

One skilled in the art would not interpret the mixing quad formed by transistors Q3, Q4, Q5 and Q6 (much less the artificial combination of transistors Q3 and Q6 taken alone) as an "input stage" as recited in claim 15. This is born out by the Voinigescu reference itself, which distinguishes between an input stage (see col. 14, lines 29-30 referring to transistors Q1 and Q2 in Fig. 9 as an "input pair") and a mixing quad (see col. 14, lines 31-32). This is also supported by the entirety of Applicant's specification, which consistently distinguishes between a mixer core and an input stage. (See, e.g., page 5, line 27 of the specification referring to the mixer core 24 and input section 26 of Fig. 3.)

Additional evidence of the conceptual separation of the mixing core and other stages can be found in the article "Low Voltage Performance of a Microwave CMOS Gilbert Cell Mixer", *IEEE Journal of Solid-State Circuits* by P.J. Sullivan, B.A. Xavier and W.H. Ku, Vol. 32, No. 7, July 1997, pp. 1151-1155 (the "Sullivan article"). For example, the Sullivan article refers to an "amplifier section" (page 1151, second column, third line from bottom) (note that claim 15 is drawn to an "amplifier cell") and a "mixer core" (page 1152, second column, second line from bottom).

Thus, Voinigescu does not disclose a second input stage as recited in claim 15.

Claim 15 also recites a first class AB input stage coupled to the first and second output terminals and arranged to drive the first and second output terminals responsive to a first input signal. The examiner alleges that transistors Q1 and Q2 in Fig. 9 of Voinigescu satisfy this limitation. Applicant concedes that transistors Q1 and Q2 form an input stage. However, it is not a class AB input stage, and it is not arranged as recited in claim 15 if one accepts the Examiner's interpretation of Voinigescu's IF- and IF+ terminals as being the first and second output terminals.

The Examiner acknowledges that Voinigescu does not disclose class AB input stages, but alleges that Mitzlaff provides the motivation to modify Voinigescu to use class AB input stages "for higher efficiency when in FM operation". As discussed above, Voinigescu does not teach two input stages arranged as recited in claim 15, and therefore, cannot serve as a basis for modification according to the teachings of Mitzlaff. Nonetheless, assuming for the sake of argument that the Examiner's analysis of Voinigescu is correct, Mitzlaff does not teach the desirability of using any particular type of input stage. Rather, Mitzlaff simply discloses the

benefit *of driving an input stage into saturation* regardless of whether the input stage is class A, class AB, etc. (Col. 2, line 62-66.) Thus, Mitzlaff does not provide any suggestion or motivation to combine the references, and a *prima facie* case of obviousness has not been established.

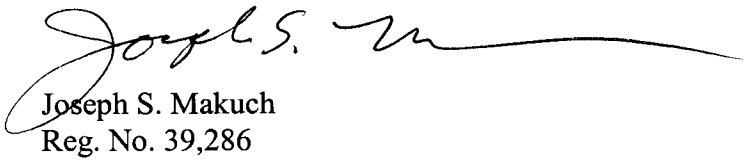
In the Final Office Action (Paper No. 23) mailed June 4, 2004, the Examiner summarily dismissed Applicant's arguments and stated that they are not relevant because claim 15 does not recite a mixer core. As best understood by applicant, the Examiner seems to be arguing that, since claim 15 does not recite a mixer core, there is no need to distinguish between input stages and mixer cores in the prior art. But such a position is inconsistent with the axiom that claims are presumed to have the meaning attributed to them by those of ordinary skill in the art. As established above, input stages and mixer cores are understood to be different things to those of ordinary skill in the art. To interpret components of a mixer core as an input stage is an unreasonable interpretation. Moreover, the Examiner's tersely worded statement fails to explain how the interrelation of components recited in claim 15 would be satisfied under the Examiner's interpretation of claim terms.

CONCLUSION

Applicant requests that the rejection of claim 15 be reversed.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



Joseph S. Makuch
Reg. No. 39,286

MARGER JOHNSON & McCOLLOM, P.C.
210 SW Morrison Street, Suite 400
Portland, OR 97204
(503) 222-3613

CLAIMS APPENDIX

The claim involved in the appeal read as follows:

15. (Rejected) An amplifier cell comprising:

first and second input terminals;

first and second output terminals;

first class AB input stage coupled to the first and second output terminals and arranged to drive the first and second output terminals responsive to a first input signal received at the first input terminal; and

a second class AB input stage coupled to the first and second output terminals and arranged to drive the first and second output terminals responsive to a second input signal received at the second input terminal.

EVIDENCE APPENDIX

Copies of the following references are attached:

U.S. Patent No. 5,789,799 to Voinigescu et al. ("Voinigescu") entered in the record through form PTO-892 as part of Paper No. 6, mailed March 28, 2001.

U.S. Patent No. 5,307,512 to Mitzlaff ("Mitzlaff") entered in the record through form PTO-892 as part of Paper No. 6, mailed March 28, 2001.

"Low Voltage Performance of a Microwave CMOS Gilbert Cell Mixer", *IEEE Journal of Solid-State Circuits* by P.J. Sullivan, B.A. Xavier and W.H. Ku, Vol. 32, No. 7, July 1997, pp. 1151-1155 (the "Sullivan article") entered in the record through IDS and form 1449 filed March 11, 2004.

RELATED PROCEEDINGS APPENDIX

None.